AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-2. (canceled)

3. (currently amended) A semiconductor device comprising a signal transmission line and a plurality of repeaters inserted in said signal transmission line to divide said signal transmission line into a plurality of divided signal lines, each of said repeaters comprising first and second logic gates cascaded in this order along a direction of a signal transmission in said signal transmission line, each of said first and second logic gates having a logic inverting function, said first logic gate having a current driveability larger than a current driveability of said second logic gate.

4. (currently amended) The semiconductor device according to claim 3, wherein each of said divided signal lines is longer than an internal signal line connecting together said first and second inverters in each of said ~~repeater~~ repeaters.

5. (currently amended) The semiconductor device according to claim 3, further comprising a branch signal line and another

repeater having an input connected to said branch line, said another repeater comprising third and fourth logic gates cascaded in this order and having a logic inverting function, said third logic gate having a current driveability larger than a current driveability of said fourth logic gate, one of said repeaters having an output connected to an input of another of said repeaters through one of said divided signal lines and said another repeater through said branch signal line.

6. (original) The semiconductor device according to claim 5, wherein said signal transmission line is a clock distribution line.

7. (new) The semiconductor device of claim 3, wherein each of said divided signal lines has a higher capacitance than an input capacitance of a respective one of said repeaters connected thereto.

8. (new) A semiconductor device, comprising:

a first functional block connected to a second functional block by a signal transmission line;

plural repeaters in said signal transmission line that divide said signal transmission line into plural divided signal lines, each of said divided signal lines having a higher

capacitance than an input capacitance of a respective one of said repeaters connected thereto; and

each of said plural repeaters comprising first and second logic gates, said first logic gate preceding said second logic gate in a direction of transmission of a signal in said signal transmission line, and said first logic gate having a current driveability larger than a current driveability of said second logic gate.